3302A, 3302A-4, 3302AL6, 3322A, 3322A-4, 3322AL6

HIGH SPEED 2048 BIT READ ONLY MEMORY

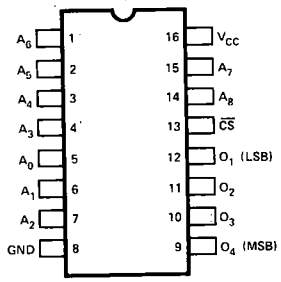
- **Fast Access Time—70ns (3302A, 3322A) Over Temperature and Supply Voltage Variation**
- **Low Standby Power Dissipation (3302AL6) — 115 μW/bit**
- **Fully Decoded—on Chip Address Decode and Buffer**
- **DTL and TTL Compatible—Input Loading is 0.25 mA max—Output Sink is 15 mA**
- **Open Collector (3302A, 3302A-4, 3302AL6) and Three State (3322A, 3322A-4, 3322AL6) Outputs**
- **Simple Memory Expansion—Single Chip Select Input Lead**
- **Standard Packaging—16 Pin Dual In-Line Lead Configuration**

The 3302A and 3322A device families are high density 2048 bit (512 words by 4-bit) ROMs. Electrical performance is specified over the complete ambient temperature range 0°C to 75°C and V_{CC} supply voltage range of 5V ±5%. The 3302A and 3322A ROM families are pin compatible with the Intel® 3602 and 3622 PROM families. Consequently initial circuit prototyping can be performed using the pin compatible PROMs.

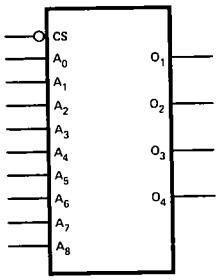
The 3302A-4 and 3322A-4 are ideal for slower performance systems (>90 ns) where low system cost is a prime factor. For those systems requiring low power dissipation, one should consider the 3302AL6/3322AL6. Not only does the 3302AL6/3322AL6 dissipate 20% less active power than the 3302/3322, but it also has an added low standby power dissipation feature. Whenever the 3302AL6/3322AL6 is deselected, power dissipation is reduced by 70%.

The 3302A and 3322A device families are manufactured using Schottky barrier diode clamped transistors which results in higher speed performance than equivalent devices made with gold diffusion process.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC1}	Power Supply Current (3302, 3302-4, 3322, 3322-4)			140	mA	V_{CC} = 5.25V, V_{A0} - V_{A8} = 0V, $\overline{CS}$ = 0V
I_{CC2}	Power Supply Current (3302L-6, 3322L-6) Active			110	mA	V_{CC} = 5.25V, $\overline{CS}$ = 0.45V
	Standby			45	mA	$\overline{CS}$ = 2.4V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3322A, 3322A-4, 3322AL6 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	µA	V_O = 5.25V or 0.45V, V_{CC} = 5.25V, $\overline{CS}$ = 2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC} = 5.00V, T_A = 25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMIT 3302A 3322A	MAX. LIMIT 3302A-4 3322A-4	MAX. LIMIT 3302AL6 3322AL6	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	70	90	90	ns	$\overline{CS}$ = V_{IL} to Select the ROM
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	120	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

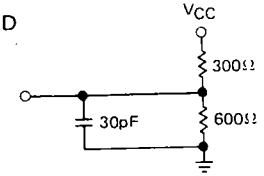
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

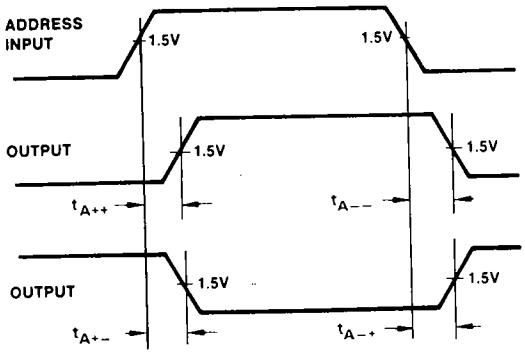
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

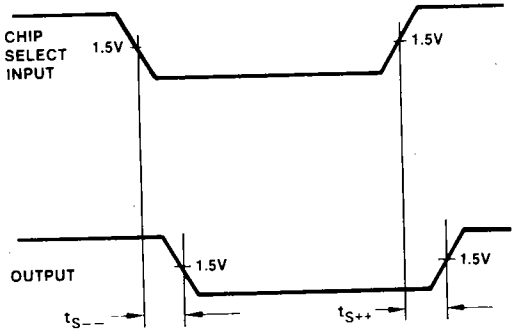


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



ROMs